IN THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1(Currently Amended). A signal processing system comprising:

a scale reduced Fast Fourier Transform component configured to transform ~~transforming~~ an input signal from the time domain to the frequency domain; and, ~~the scale reduced Fast Fourier Transform component having a plurality of processing stages with scaling associated with stages to compensate for bit growth, such scaling being omitted at stages where bit growth is absent due to characteristics of the input signal.~~

a signal analyzer configured to

perform a first summation of input magnitudes for N points of the input signal to determine a total number of bits that an output signal grows,

perform a second summation of input magnitudes on at least one stage of a N-point Fast Fourier Transform to determine which of a plurality of processing stages of the scale reduced Fast Fourier Transform component experience bit growth, and

compare the first summation with the second summation to verify appropriate scaling has been determined.

2(Original). The system of claim 1, the plurality of processing stages being a plurality of complex additions and complex multiplications.

3(Original). The system of claim 2, the plurality of processing stages comprising at least one radix-M stage where M is an integer greater than zero.

4(Original). The system of claim 2, the plurality of processing stages comprising at least one of a radix-2 stage and a radix-4 stage.

5(Original). The system of claim 2, the plurality of processing stages comprising an output scaling stage to compensate for scaling of stages due to bit growth at the corresponding stage and to provide a desired scaled output.

6(Currently Amended). The system of claim 1, wherein the signal analyzer is further configured to ~~further comprising a signal analyzer that analyzes~~ analyze the characteristics of the input signal and ~~determines~~ determine which of ~~the~~ a plurality of processing stages experience bit growth, the signal analyzer providing scaling at the processing stages that experience bit growth, such scaling being omitted at stages where bit growth is absent due to the characteristics of the input signal.

7. Canceled.

8(Original). The system of claim 1, the scale reduced Fast Fourier Transform component residing in a channel estimator and providing a channel estimate derived from a channel impulse response.

9(Currently Amended). A channel estimator comprising:

a training tone extractor operative to extract training tones from a digitized data signal;

an Inverse Fast Fourier Transform component that determines a channel impulse response based on the extracted training tones; ~~and~~

a Fast Fourier Transform component that transforms the channel impulse response into a channel estimate, the Fast Fourier Transform component having a plurality of processing stages with scaling provided at stages to compensate for bit growth, such scaling being omitted at stages where bit growth is absent due to the characteristics associated with the channel impulse response[[.]];and

a signal analyzer configured to

perform a first summation of input magnitudes for N points of the input signal to determine a total number of bits that an output signal grows,

perform a second summation of input magnitudes on at least one stage of a N-point Fast Fourier Transform to determine which of the plurality of

processing stages of the scale reduced Fast Fourier Transform component experience bit growth, and

compare the first summation with the second summation to verify appropriate scaling has been determined.

10(Original). The channel estimator of claim 9, the Fast Fourier Transform component performing a N-point Fast Fourier Transform on the channel impulse response and the plurality of processing stages being $Log_2(N)$ number of radix-2 stages.

11(Original). The channel estimator of claim 10, N being 128 and $Log_2(N)$ number of radix-2 stages being 7.

12(Original). The channel estimator of claim 11, the channel impulse response having amplitude values that are substantially zero where scaling is provided to compensate for bit growth between the third stage and fourth stages and omitted at other stages.

13(Original). The channel estimator of claim 11, the second and third radix-2 stages, the fourth and fifth radix-2 stages and the sixth and seventh radix-2 stages comprising a first, a second and a third radix-4 stage, respectively.

14(Original). The channel estimator of claim 9, the data signal being transmitted in a multicarrier modulation format.

15(Original). The channel estimator of claim 9, at least a portion of the channel estimator residing on a digital signal processor.

16(Currently Amended). A modem for communicating over a transmission channel, the modem comprising:

a front end portion operable to receive data encoded in time domain data signals having a generally consistent format; and

a digital signal processor coupled to the front end portion, the digital signal processor being programmed to perform a N-point Fast Fourier Transform on the time

domain data signals to convert the time domain data signals into frequency domain data signals, the N-point Fast Fourier Transform having a plurality of processing stages with scaling provided at stages where bit growth is present and scaling being omitted from stages where bit growth is absent, the stages with and without bit growth being determined by analyzing the general consistent format of the time domain data signals[[.]], wherein the digital signal processor is further configured to

perform a first summation of input magnitudes for N points of the input signal to determine a total number of bits that an output signal grows,

perform a second summation of input magnitudes on at least one stage of a N-point Fast Fourier Transform to determine which of the plurality of processing stages of the scale reduced Fast Fourier Transform component experience bit growth, and

compare the first summation with the second summation to verify appropriate scaling has been determined.

17(Original). The modem of claim 16, the analyzing of the general consistent format being performed by modeling and simulation prior to programming of the digital signal processor.

18(Original). The modem of claim 16, the analyzing of the general consistent format being performed by a signal analyzer routine that determines scaling in real-time and stores the scaling in memory for subsequent time domain data signals.

19(Original). The modem of claim 16, the data signal being transmitted in a multicarrier modulation format and the modem being a wireless modem.

20.(Currently Amended). A receiver system, comprising:

means for receiving at least one digitized signal in the time domain; ~~and~~

means for performing a N-point Fast Fourier Transform on the at least one digitized signal to convert the at least one digitized signal to the frequency domain, the N-

point Fast Fourier Transform having scaling associated with those of a plurality of processing stages where bit growth is present and having no scaling at stages where bit growth is absent[[.]]; and

means for performing a first summation of input magnitudes for N points of the input signal to determine a total number of bits that an output signal grows, performing a second summation of input magnitudes on at least one stage of the means for performing the N-point Fast Fourier Transform to determine which of the plurality of processing stages experience bit growth, and comparing the first summation with the second summation to verify appropriate scaling has been determined.

21(Original). The system of claim 20, further comprising means for determining stages at which scaling is to be provided and omitted.

22. Canceled.

23 (Currently Amended). A method of reducing scaling in at least one Fast Fourier Transform computation being performed on signals in a wireless communication system, the method comprising:

analyzing a digitized data signal to determine Fast Fourier Transform input magnitudes for N points of the digitized signal;

summing the digitized signal input magnitudes for the N points to provide a total magnitude summation;

performing an input magnitude summation on at least one stage of a Fast Fourier Transform to determine stages at which bit growth is present and absent; ~~and~~

providing scaling at stages where bit growth is present[[.]]; and

comparing the scaling at stages where bit growth is present with the total magnitude summation to verify that the appropriate scaling has been provided.

24(Original). The method of claim 23, further comprising storing scaling values for performing a scale reduced Fast Fourier Transform on subsequent digitized data signals.

25. Canceled.

26(Currently Amended). A method for performing a channel estimation procedure comprising:

extracting training tones from a digitized data burst;

determining a channel impulse response based on the extracted training tones; ~~and~~

performing a scale reduced Fast Fourier Transform on the channel impulse response to provide a channel estimate indicative of the effects of a channel on the digitized data burst[[.]];

determining a first summation of the magnitudes of the total number of bits that a N-point Fast Fourier Transform output grows;

performing an input magnitude summation on at least one stage of the N-point Fast Fourier Transform to determine which of a plurality of processing stages experience bit growth; and

comparing the first summation with the input magnitude summation to verify appropriate scaling has been determined.

27(Original). The method of claim 26, the scale reduced Fast Fourier Transform component having a plurality of processing stages with scaling associated with stages to compensate for bit growth, such scaling being omitted at stages where bit growth is absent due to characteristics associated with the channel impulse response.

28(Original). The method of claim 26, the data burst being transmitted in a multicarrier modulation format and the channel impulse response having a finite duration impulse response.

29(Original). The method of claim 26, further comprising analyzing the data burst and determining which of the plurality of stages experiences bit growth and providing scaling at the stages that experience bit growth.

30. Canceled.

31. Canceled.